FIG. 1

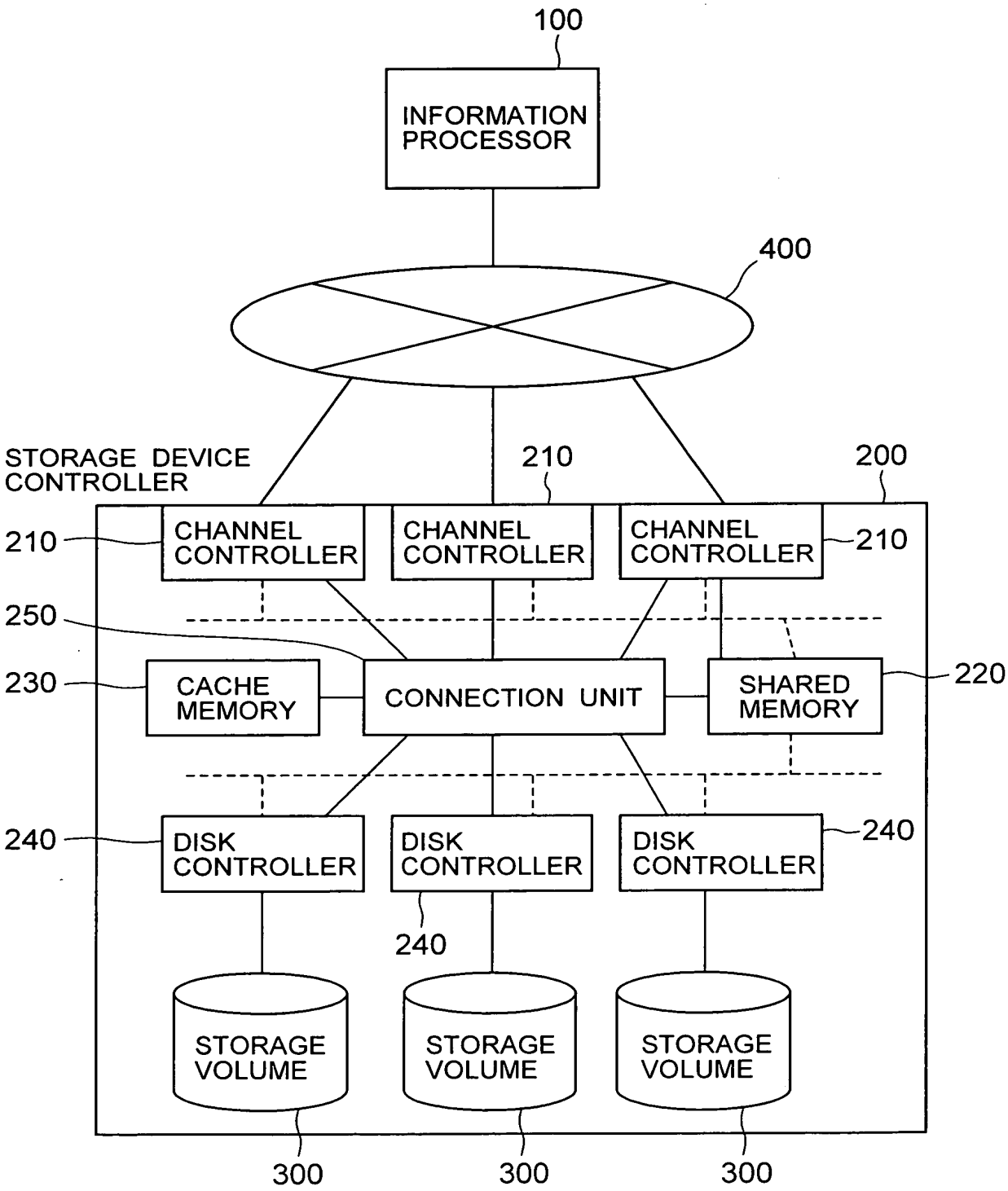

100
INFORMATION PROCESSOR
400
STORAGE DEVICE CONTROLLER
210
200
210
CHANNEL CONTROLLER
CHANNEL CONTROLLER
CHANNEL CONTROLLER
210
250
230
CACHE MEMORY
CONNECTION UNIT
SHARED MEMORY
220
240
DISK CONTROLLER
DISK CONTROLLER
DISK CONTROLLER
240
240
STORAGE VOLUME
STORAGE VOLUME
STORAGE VOLUME
300
300
300

FIG. 2

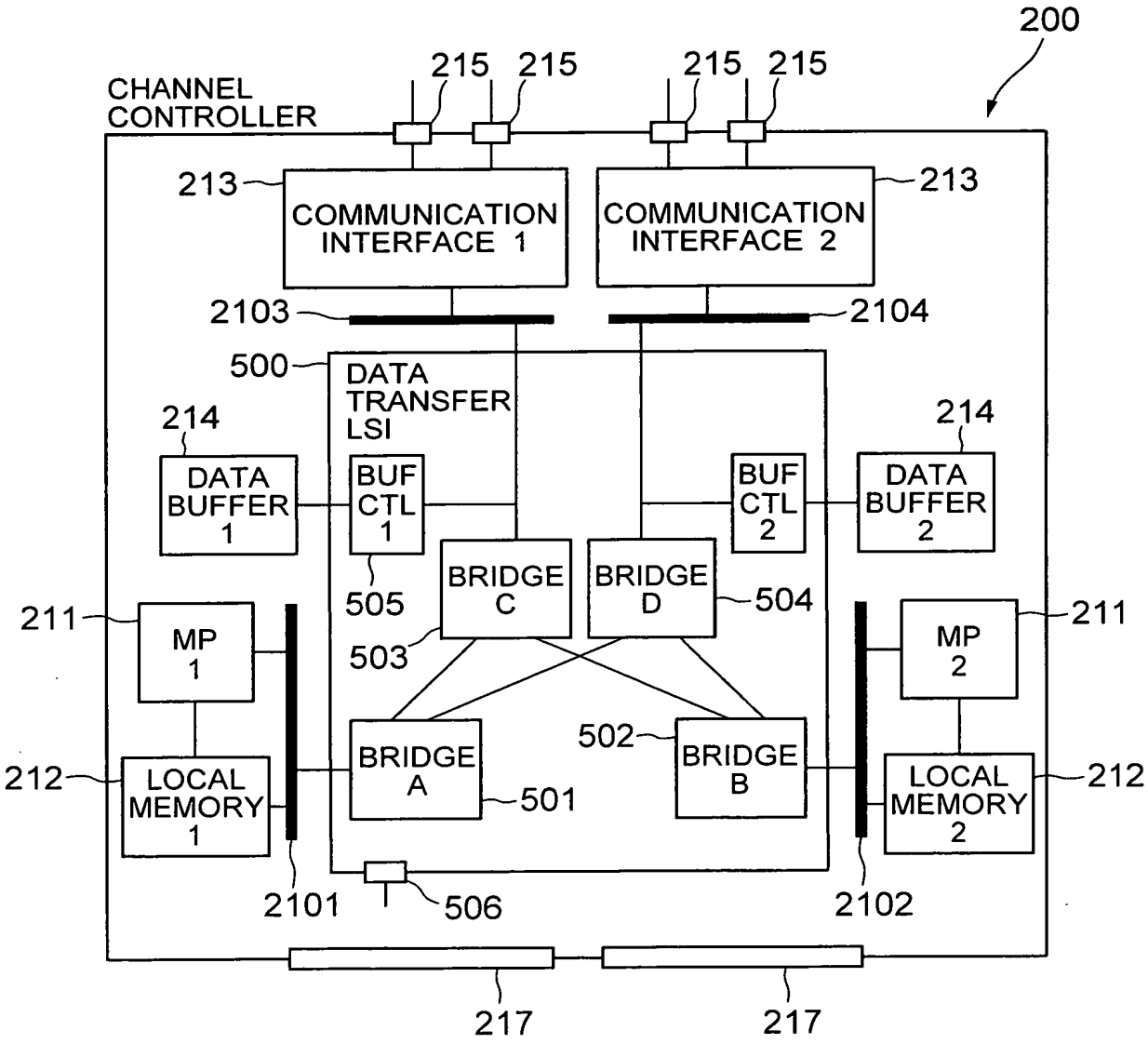

200
CHANNEL CONTROLLER
215
215
215
215
213
COMMUNICATION INTERFACE 1
COMMUNICATION INTERFACE 2
213
2103
2104
500
DATA TRANSFER LSI
214
214
DATA BUFFER 1
BUF CTL 1
BUF CTL 2
DATA BUFFER 2
505
BRIDGE C
BRIDGE D
504
503
211
MP 1
MP 2
211
212
LOCAL MEMORY 1
BRIDGE A
501
502
BRIDGE B
LOCAL MEMORY 2
212
2101
506
2102
217
217

FIG. 3

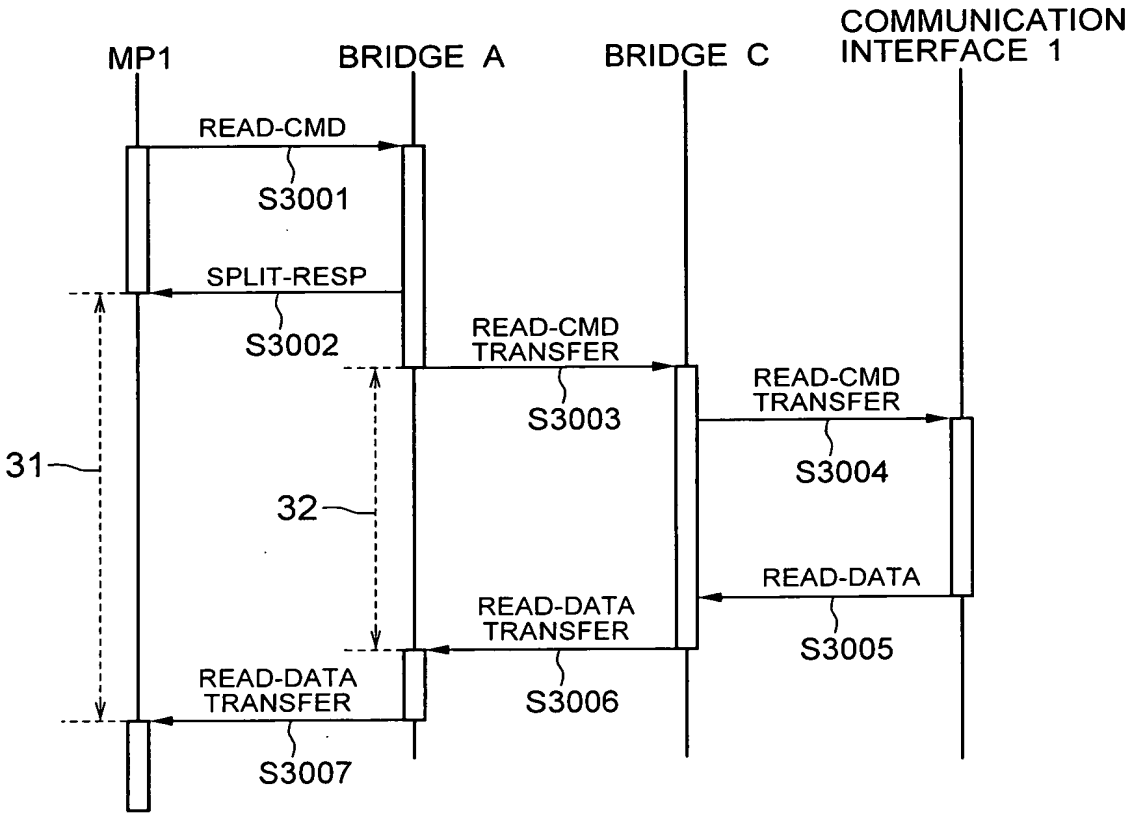

MP1
BRIDGE A
BRIDGE C
COMMUNICATION INTERFACE 1
READ-CMD
S3001
SPLIT-RESP
S3002
READ-CMD TRANSFER
S3003
READ-CMD TRANSFER
S3004
READ-DATA
S3005
READ-DATA TRANSFER
S3006
READ-DATA TRANSFER
S3007
31
32

FIG. 4

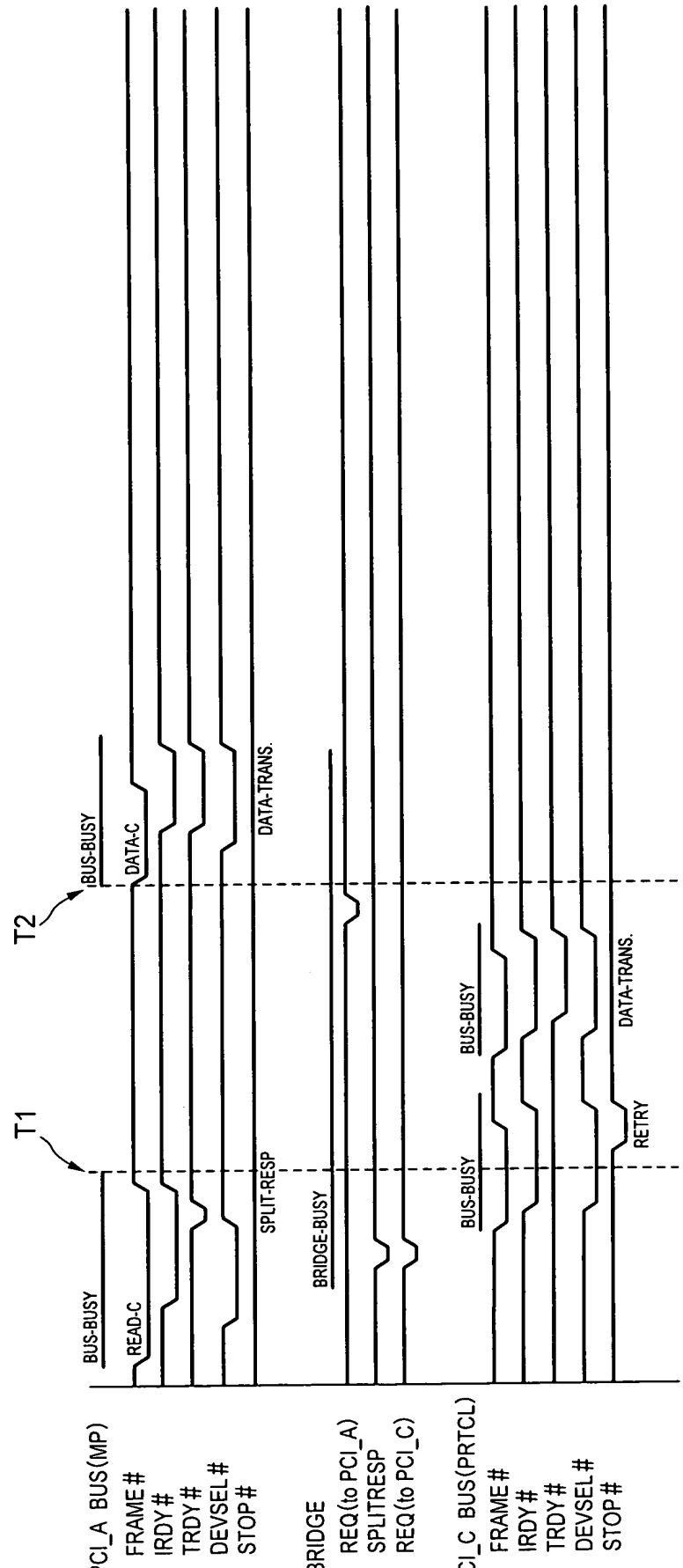

T1
T2
PCI_A BUS(MP)
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
BUS-BUSY
READ-C
SPLIT-RESP
DATA-TRANS.
BUS-BUSY
DATA-C
BRIDGE
REQ(to PCI_A)
SPLITRESP
REQ(to PCI_C)
BRIDGE-BUSY
PCI_C BUS(PRTCL)
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
BUS-BUSY
RETRY
BUS-BUSY
DATA-TRANS.

FIG. 5

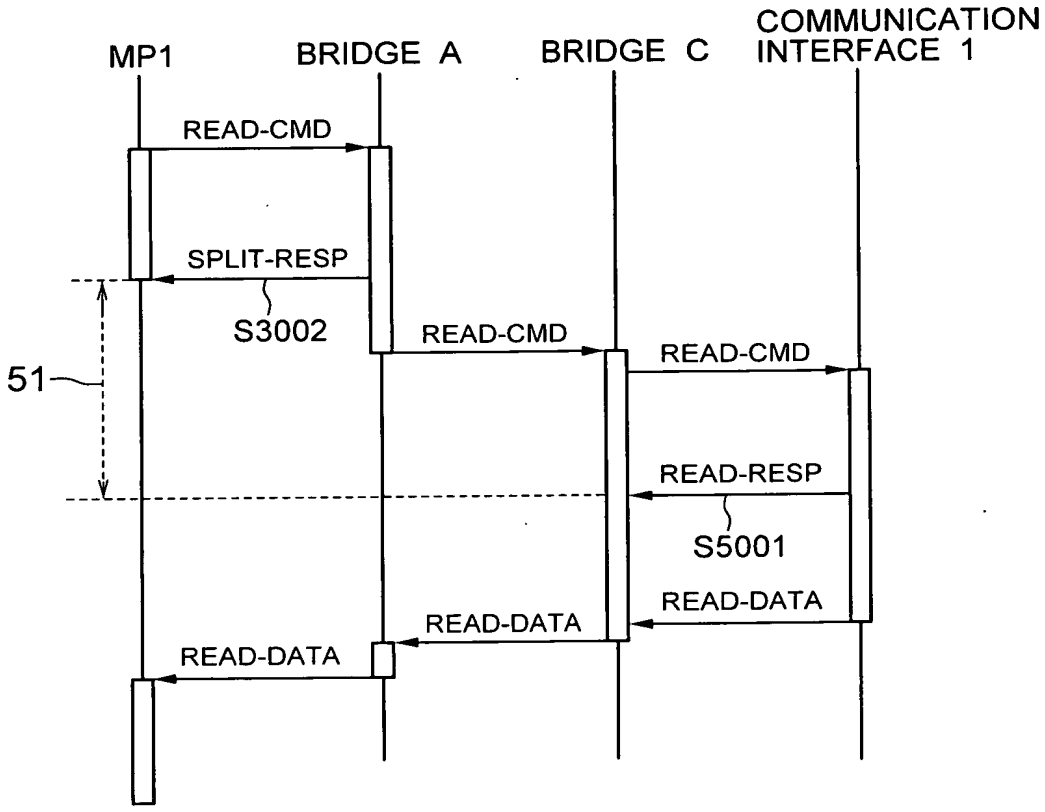

MP1
BRIDGE A
BRIDGE C
COMMUNICATION INTERFACE 1
READ-CMD
SPLIT-RESP
S3002
READ-CMD
READ-CMD
51
READ-RESP
S5001
READ-DATA
READ-DATA
READ-DATA

FIG. 6

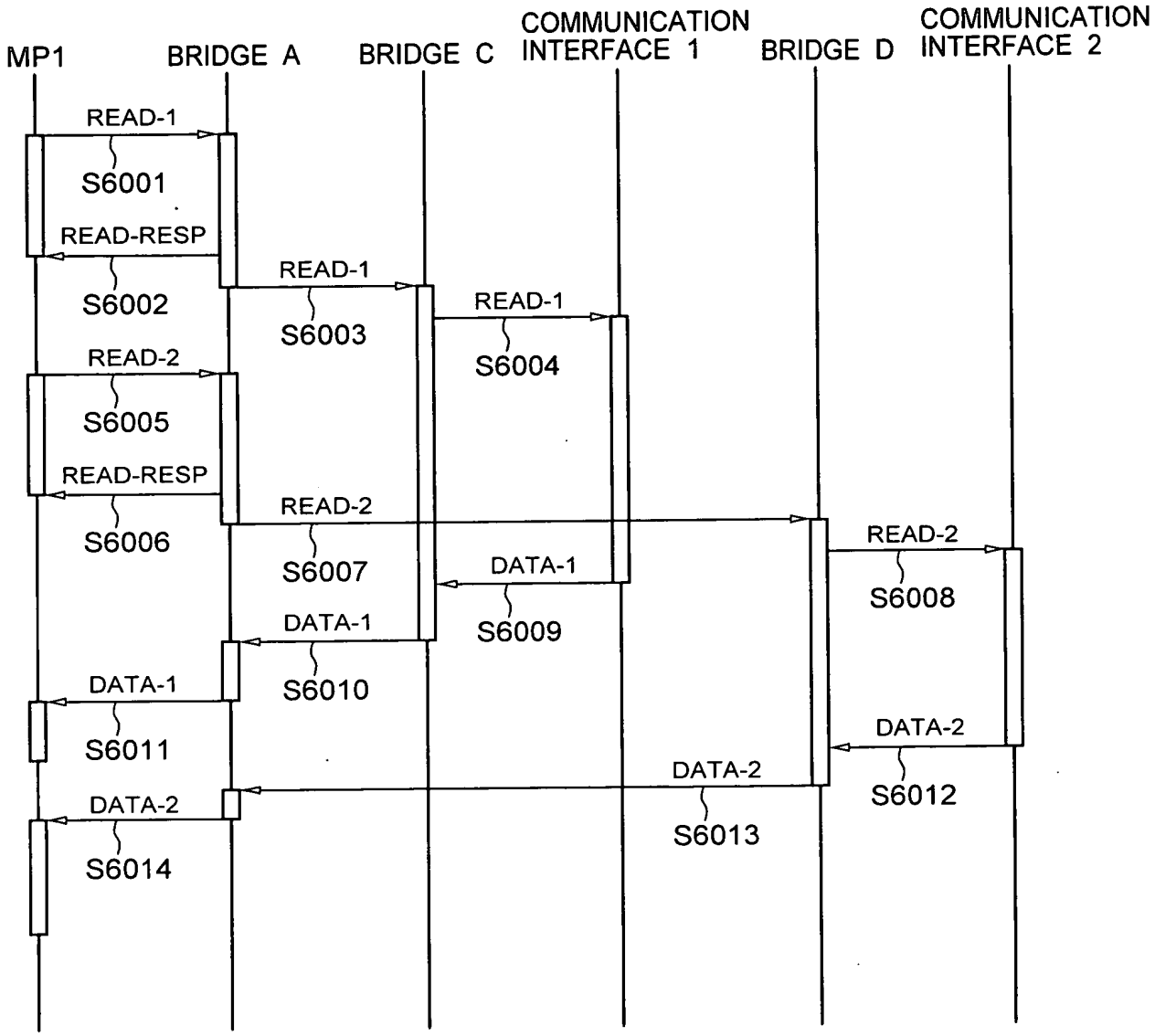

MP1
BRIDGE A
BRIDGE C
COMMUNICATION INTERFACE 1
BRIDGE D
COMMUNICATION INTERFACE 2
READ-1
S6001
READ-RESP
S6002
READ-1
S6003
READ-1
S6004
READ-2
S6005
READ-RESP
S6006
READ-2
S6007
DATA-1
S6009
READ-2
S6008
DATA-1
S6010
DATA-1
S6011
DATA-2
S6012
DATA-2
S6013
DATA-2
S6014

FIG. 7

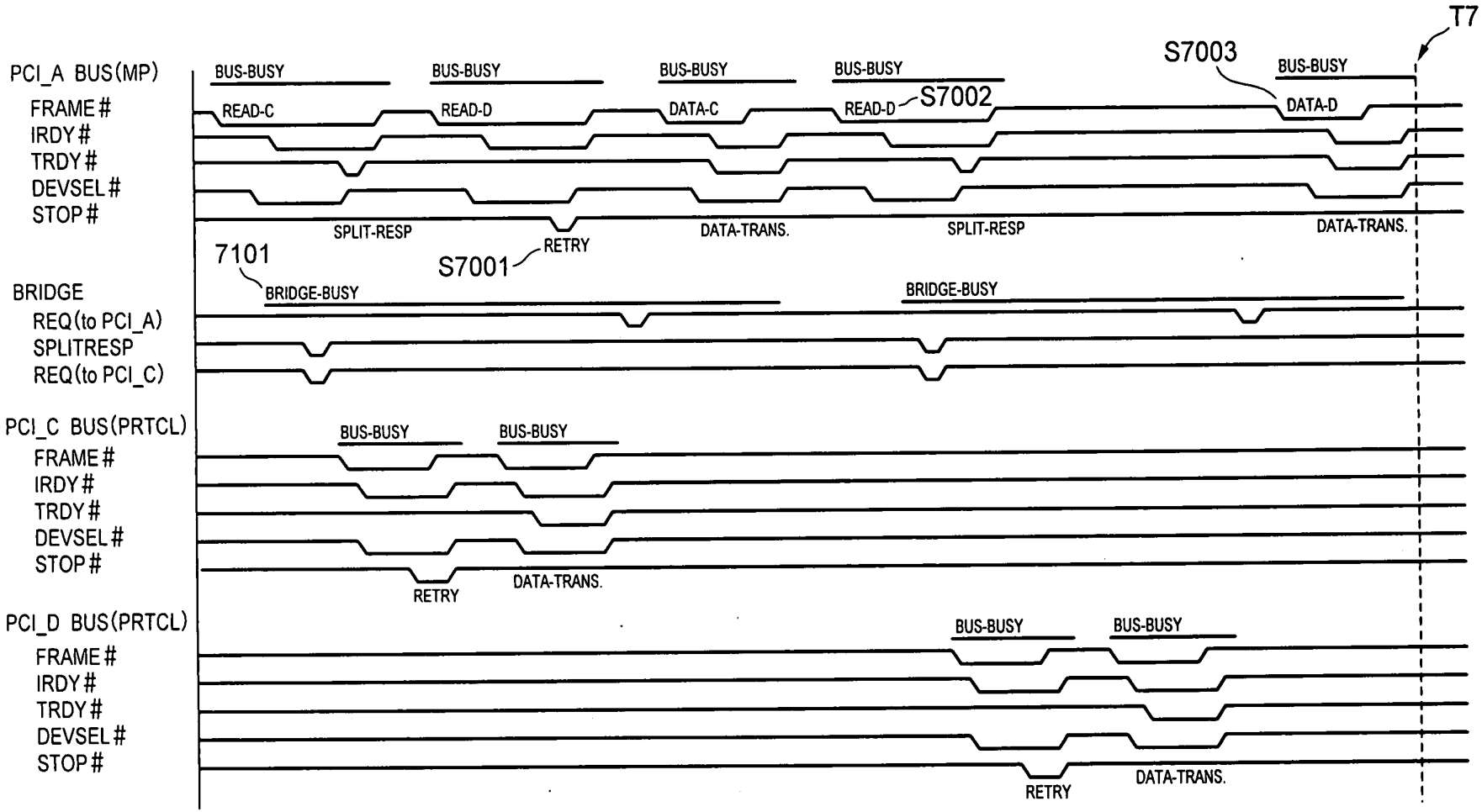

T7
S7003
PCI_A BUS(MP)
BUS-BUSY
BUS-BUSY
BUS-BUSY
BUS-BUSY
BUS-BUSY
FRAME#
READ-C
READ-D
DATA-C
READ-D
S7002
DATA-D
IRDY#
TRDY#
DEVSEL#
STOP#
SPLIT-RESP
RETRY
DATA-TRANS.
SPLIT-RESP
DATA-TRANS.
7101
S7001
BRIDGE
BRIDGE-BUSY
BRIDGE-BUSY
REQ(to PCI_A)
SPLITRESP
REQ(to PCI_C)
PCI_C BUS(PRTCL)
BUS-BUSY
BUS-BUSY
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
RETRY
DATA-TRANS.
PCI_D BUS(PRTCL)
BUS-BUSY
BUS-BUSY
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
RETRY
DATA-TRANS.

FIG. 8

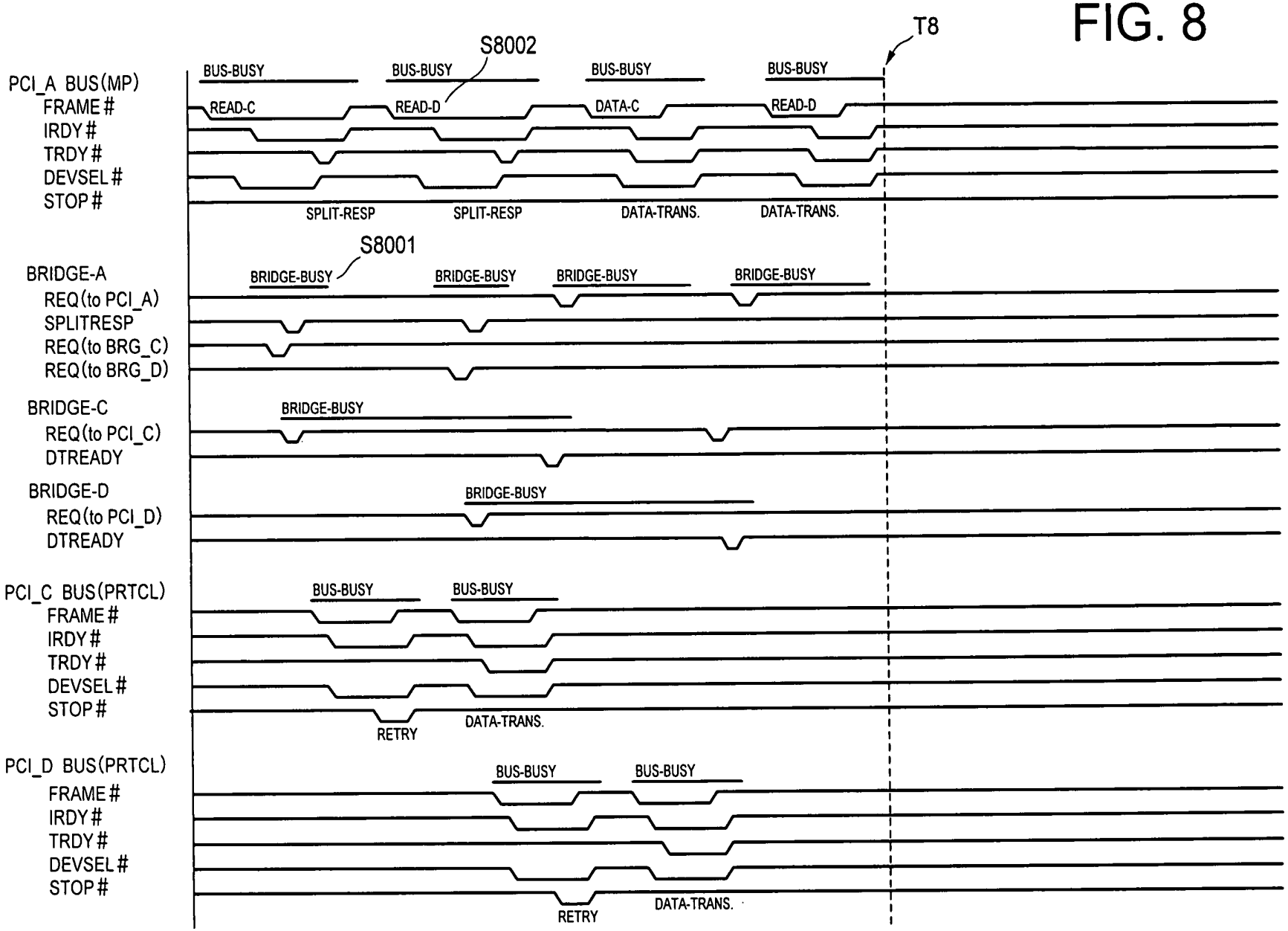

T8
S8002
PCI_A BUS(MP)
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
BUS-BUSY
BUS-BUSY
BUS-BUSY
BUS-BUSY
READ-C
READ-D
DATA-C
READ-D
SPLIT-RESP
SPLIT-RESP
DATA-TRANS.
DATA-TRANS.
S8001
BRIDGE-A
REQ(to PCI_A)
SPLITRESP
REQ(to BRG_C)
REQ(to BRG_D)
BRIDGE-BUSY
BRIDGE-BUSY
BRIDGE-BUSY
BRIDGE-BUSY
BRIDGE-C
REQ(to PCI_C)
DTREADY
BRIDGE-BUSY
BRIDGE-D
REQ(to PCI_D)
DTREADY
BRIDGE-BUSY
PCI_C BUS(PRTCL)
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
BUS-BUSY
BUS-BUSY
RETRY
DATA-TRANS.
PCI_D BUS(PRTCL)
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
BUS-BUSY
BUS-BUSY
RETRY
DATA-TRANS.

FIG. 9

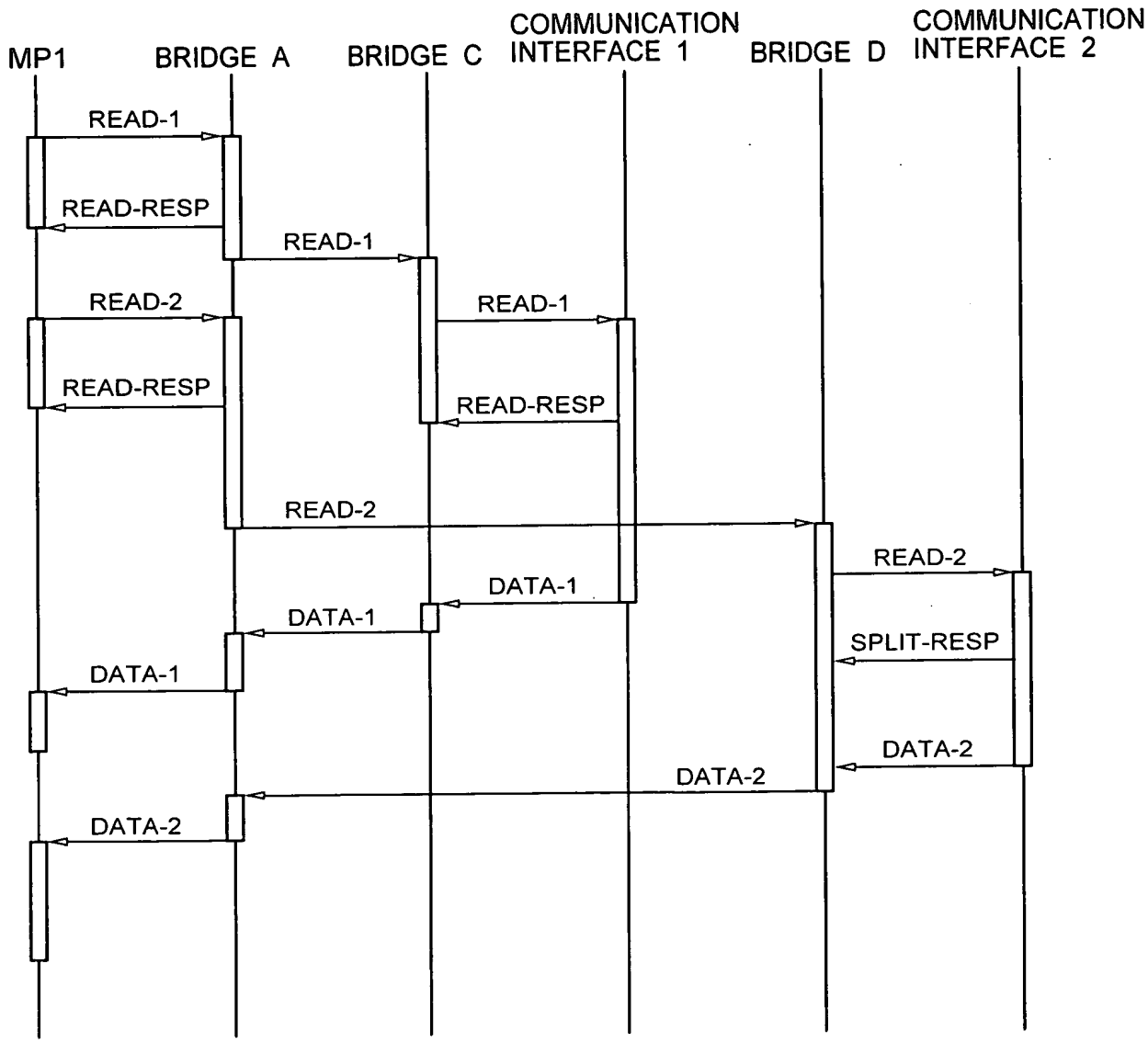

MP1
BRIDGE A
BRIDGE C
COMMUNICATION INTERFACE 1
BRIDGE D
COMMUNICATION INTERFACE 2
READ-1
READ-RESP
READ-1
READ-2
READ-1
READ-RESP
READ-RESP
READ-2
READ-2
DATA-1
DATA-1
SPLIT-RESP
DATA-1
DATA-2
DATA-2
DATA-2

FIG. 10

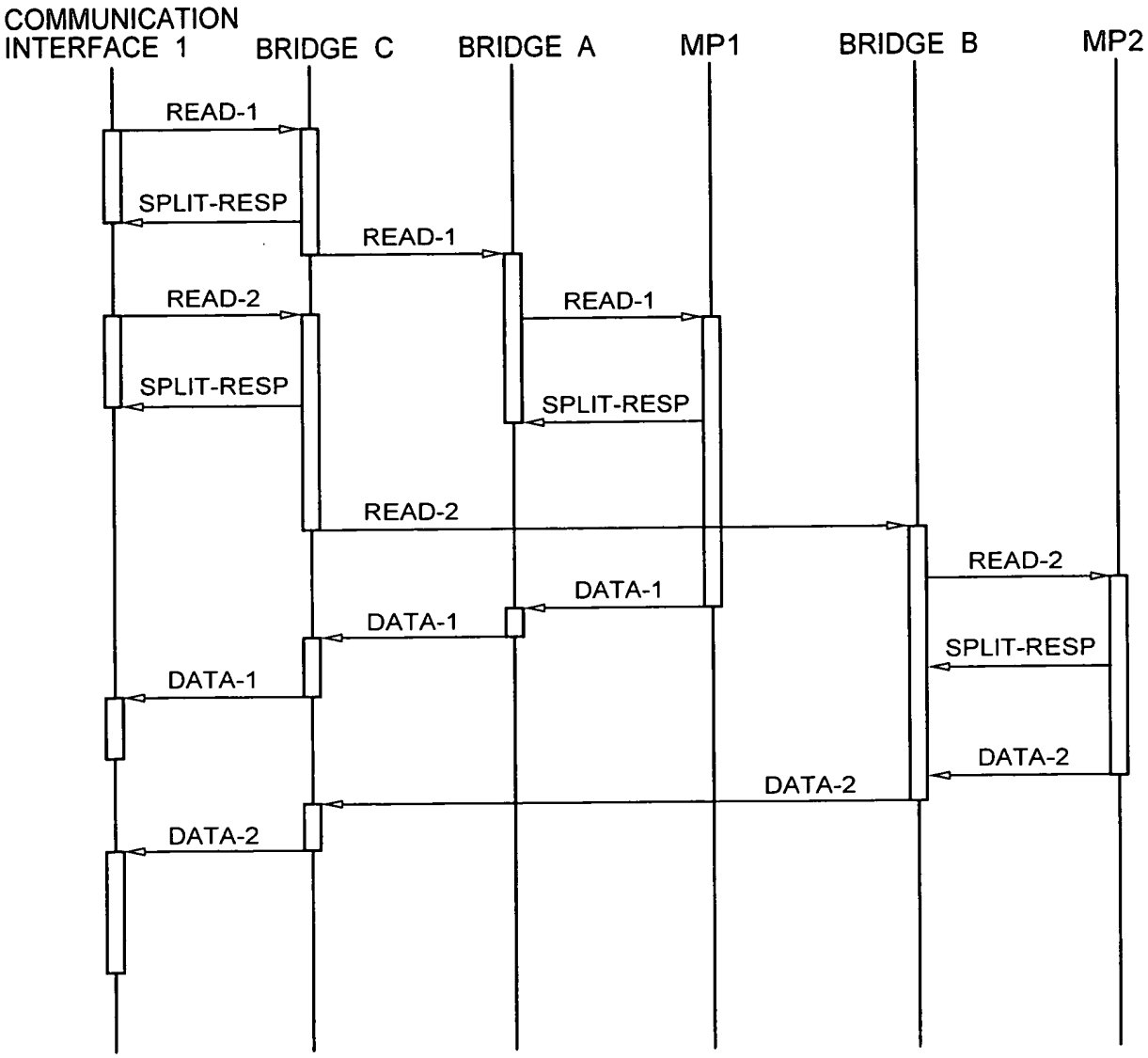

COMMUNICATION INTERFACE 1
BRIDGE C
BRIDGE A
MP1
BRIDGE B
MP2
READ-1
SPLIT-RESP
READ-1
READ-2
READ-1
SPLIT-RESP
SPLIT-RESP
READ-2
READ-2
DATA-1
DATA-1
SPLIT-RESP
DATA-1
DATA-2
DATA-2
DATA-2

FIG. 11

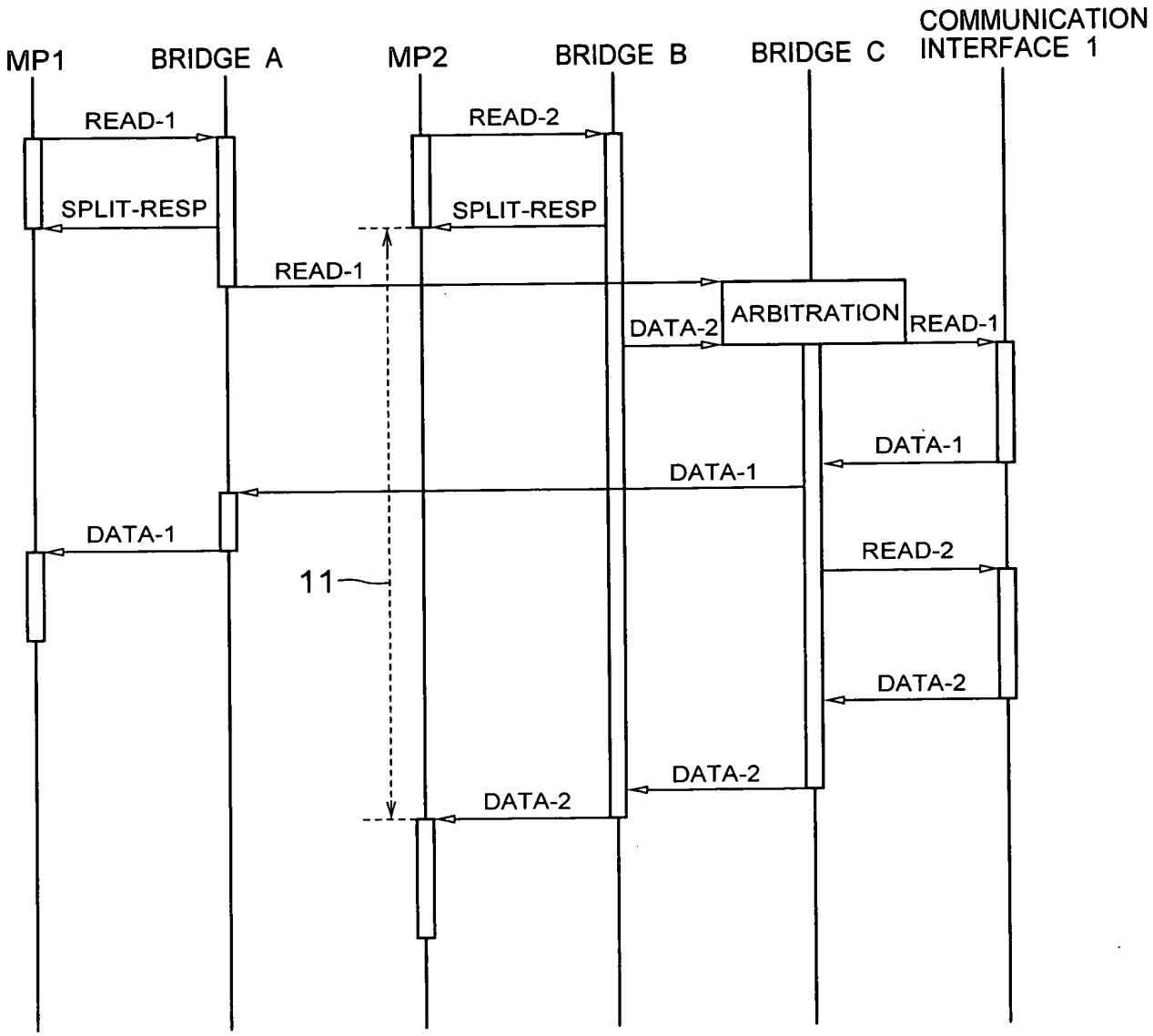

MP1
BRIDGE A
MP2
BRIDGE B
BRIDGE C
COMMUNICATION INTERFACE 1
READ-1
READ-2
SPLIT-RESP
SPLIT-RESP
READ-1
DATA-2
ARBITRATION
READ-1
DATA-1
DATA-1
DATA-1
READ-2
11
DATA-2
DATA-2
DATA-2

FIG. 12

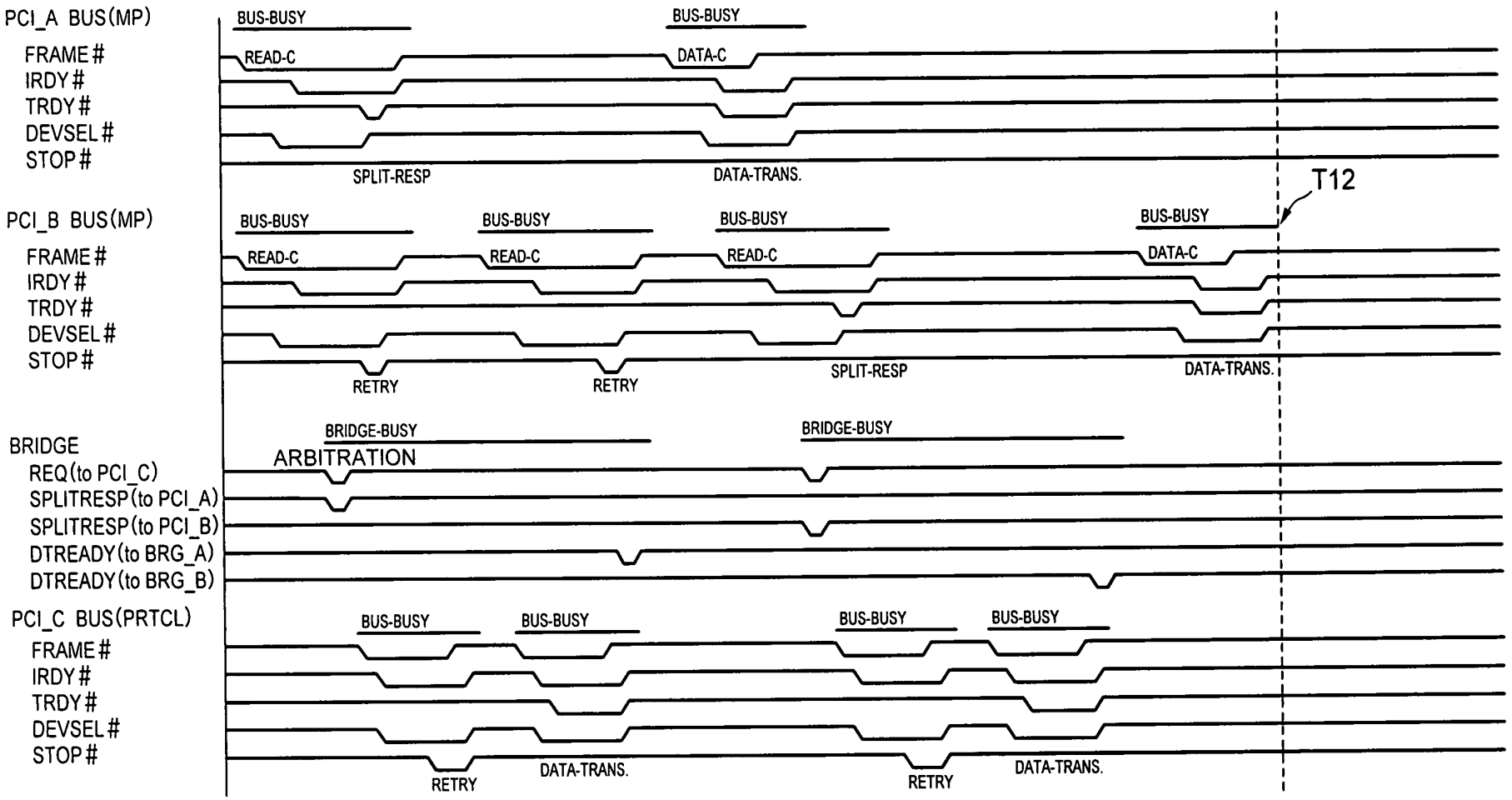

PCI_A BUS(MP)
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
BUS-BUSY
READ-C
DATA-C
SPLIT-RESP
DATA-TRANS.
T12
PCI_B BUS(MP)
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
BUS-BUSY
READ-C
DATA-C
RETRY
SPLIT-RESP
DATA-TRANS.
BRIDGE
REQ(to PCI_C)
SPLITRESP(to PCI_A)
SPLITRESP(to PCI_B)
DTREADY(to BRG_A)
DTREADY(to BRG_B)
BRIDGE-BUSY
ARBITRATION
PCI_C BUS(PRTCL)
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
BUS-BUSY
RETRY
DATA-TRANS.

FIG. 13

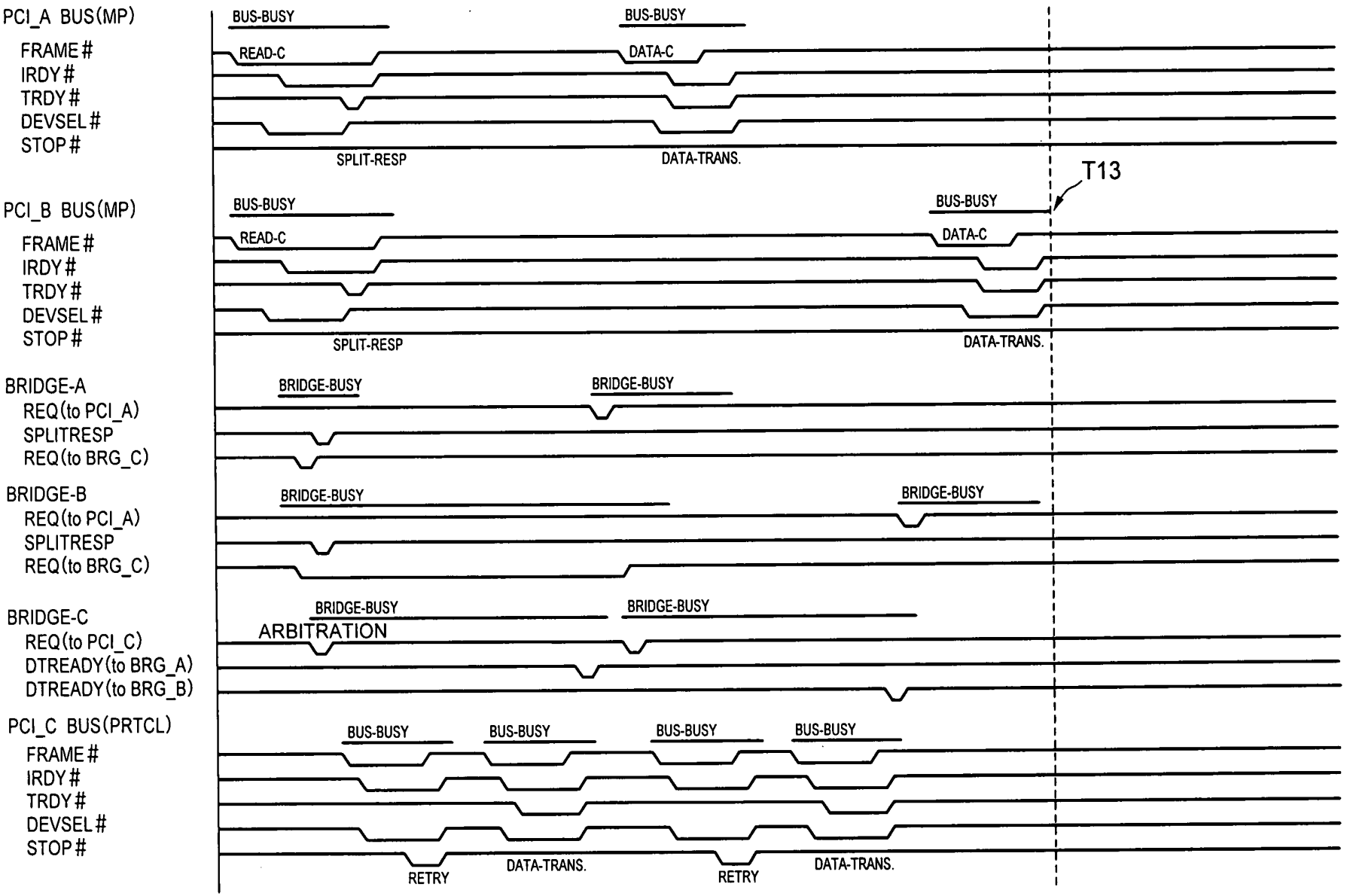

PCI_A BUS(MP)
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
BUS-BUSY
BUS-BUSY
READ-C
DATA-C
SPLIT-RESP
DATA-TRANS.
T13
PCI_B BUS(MP)
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
BUS-BUSY
BUS-BUSY
READ-C
DATA-C
SPLIT-RESP
DATA-TRANS.
BRIDGE-A
REQ(to PCI_A)
SPLITRESP
REQ(to BRG_C)
BRIDGE-BUSY
BRIDGE-BUSY
BRIDGE-B
REQ(to PCI_A)
SPLITRESP
REQ(to BRG_C)
BRIDGE-BUSY
BRIDGE-BUSY
BRIDGE-C
REQ(to PCI_C)
DTREADY(to BRG_A)
DTREADY(to BRG_B)
BRIDGE-BUSY
BRIDGE-BUSY
ARBITRATION
PCI_C BUS(PRTCL)
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
BUS-BUSY
BUS-BUSY
BUS-BUSY
BUS-BUSY
RETRY
DATA-TRANS.
RETRY
DATA-TRANS.

FIG. 14

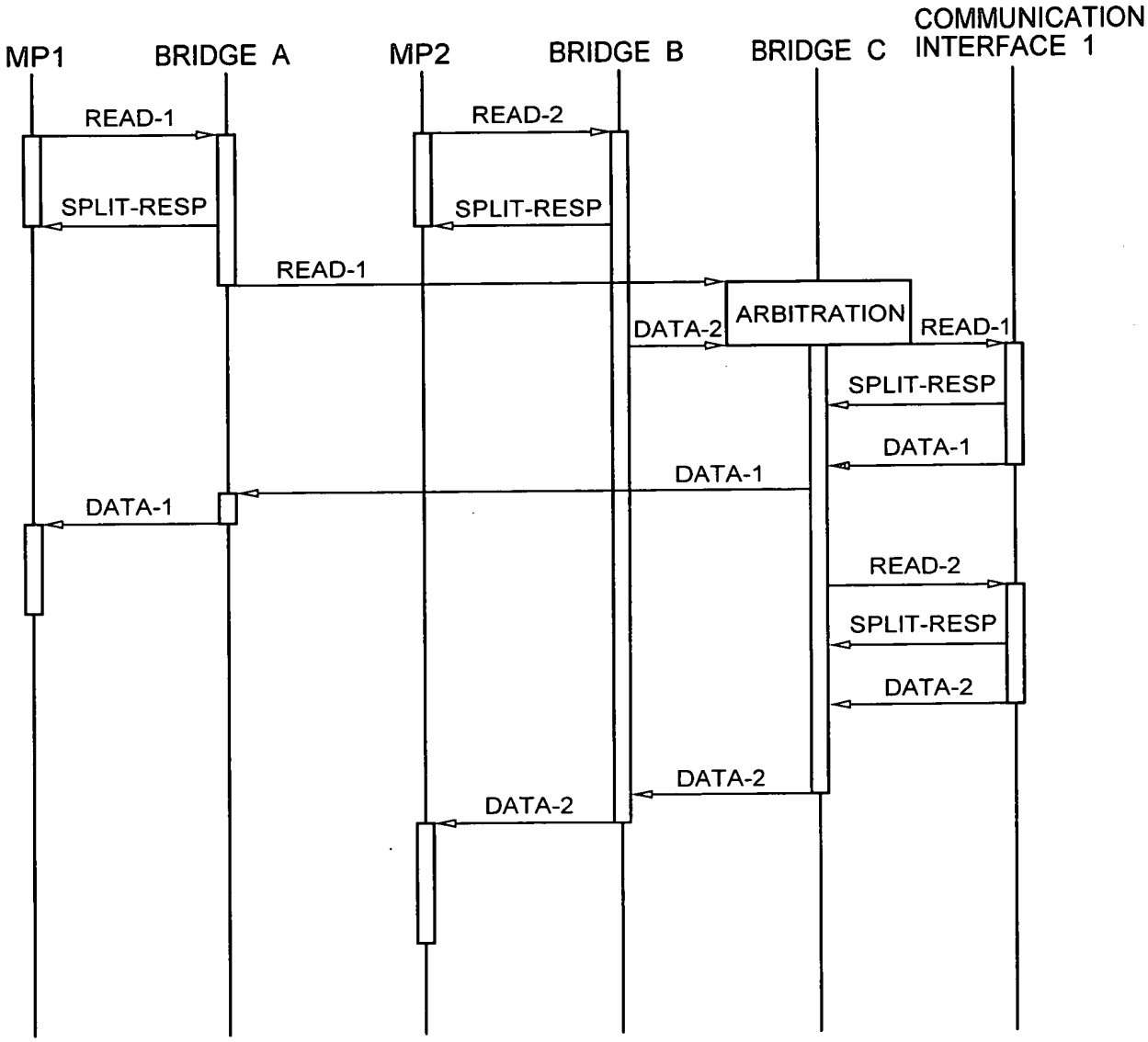

MP1
BRIDGE A
MP2
BRIDGE B
BRIDGE C
COMMUNICATION INTERFACE 1
READ-1
READ-2
SPLIT-RESP
SPLIT-RESP
READ-1
DATA-2
ARBITRATION
READ-1
SPLIT-RESP
DATA-1
DATA-1
DATA-1
READ-2
SPLIT-RESP
DATA-2
DATA-2
DATA-2

FIG. 15

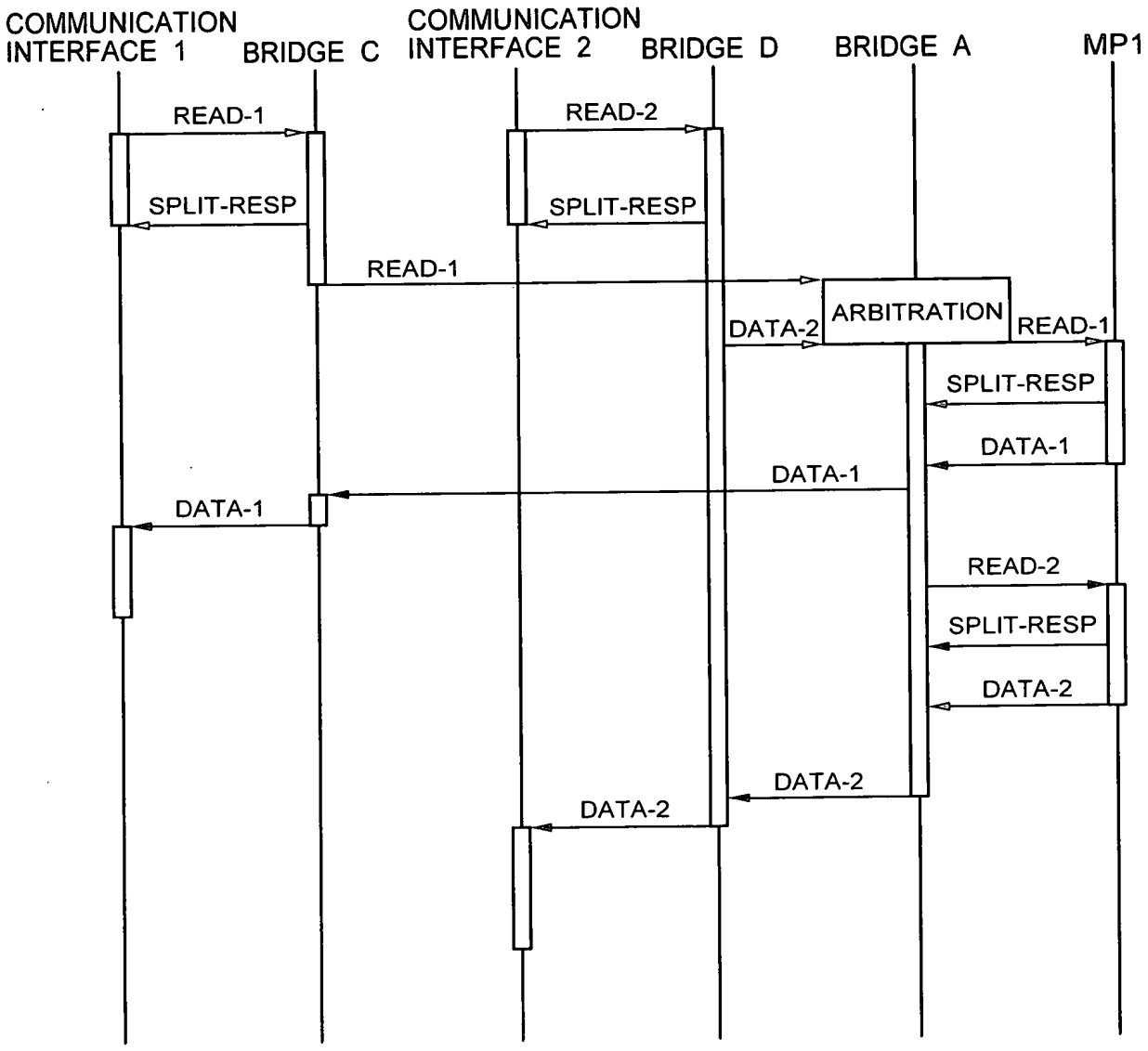

COMMUNICATION INTERFACE 1
BRIDGE C
COMMUNICATION INTERFACE 2
BRIDGE D
BRIDGE A
MP1
READ-1
READ-2
SPLIT-RESP
SPLIT-RESP
READ-1
ARBITRATION
DATA-2
READ-1
SPLIT-RESP
DATA-1
DATA-1
DATA-1
READ-2
SPLIT-RESP
DATA-2
DATA-2
DATA-2

FIG. 16

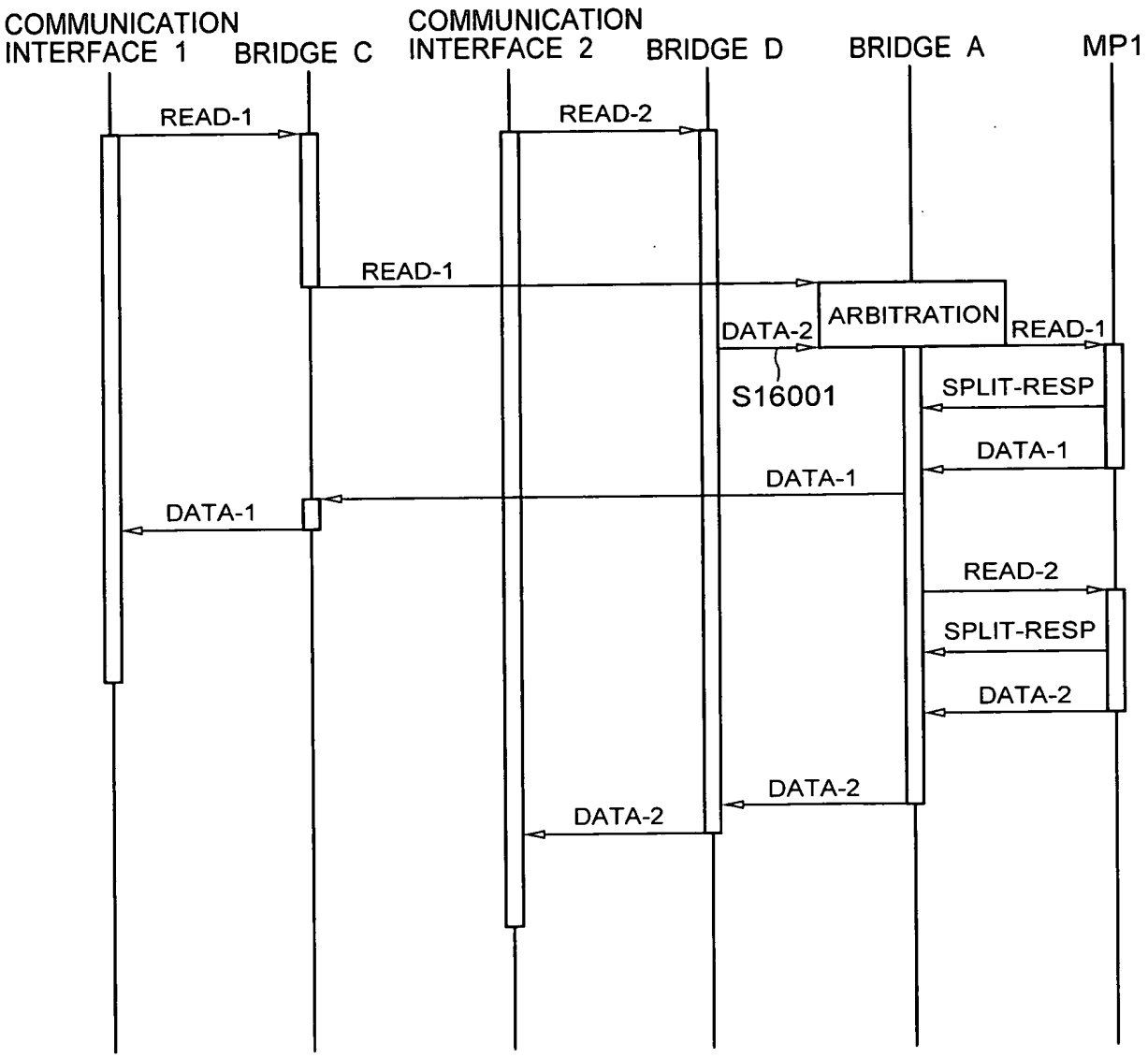

COMMUNICATION INTERFACE 1
BRIDGE C
COMMUNICATION INTERFACE 2
BRIDGE D
BRIDGE A
MP1
READ-1
READ-2
READ-1
ARBITRATION
DATA-2
READ-1
S16001
SPLIT-RESP
DATA-1
DATA-1
DATA-1
READ-2
SPLIT-RESP
DATA-2
DATA-2
DATA-2

FIG. 17

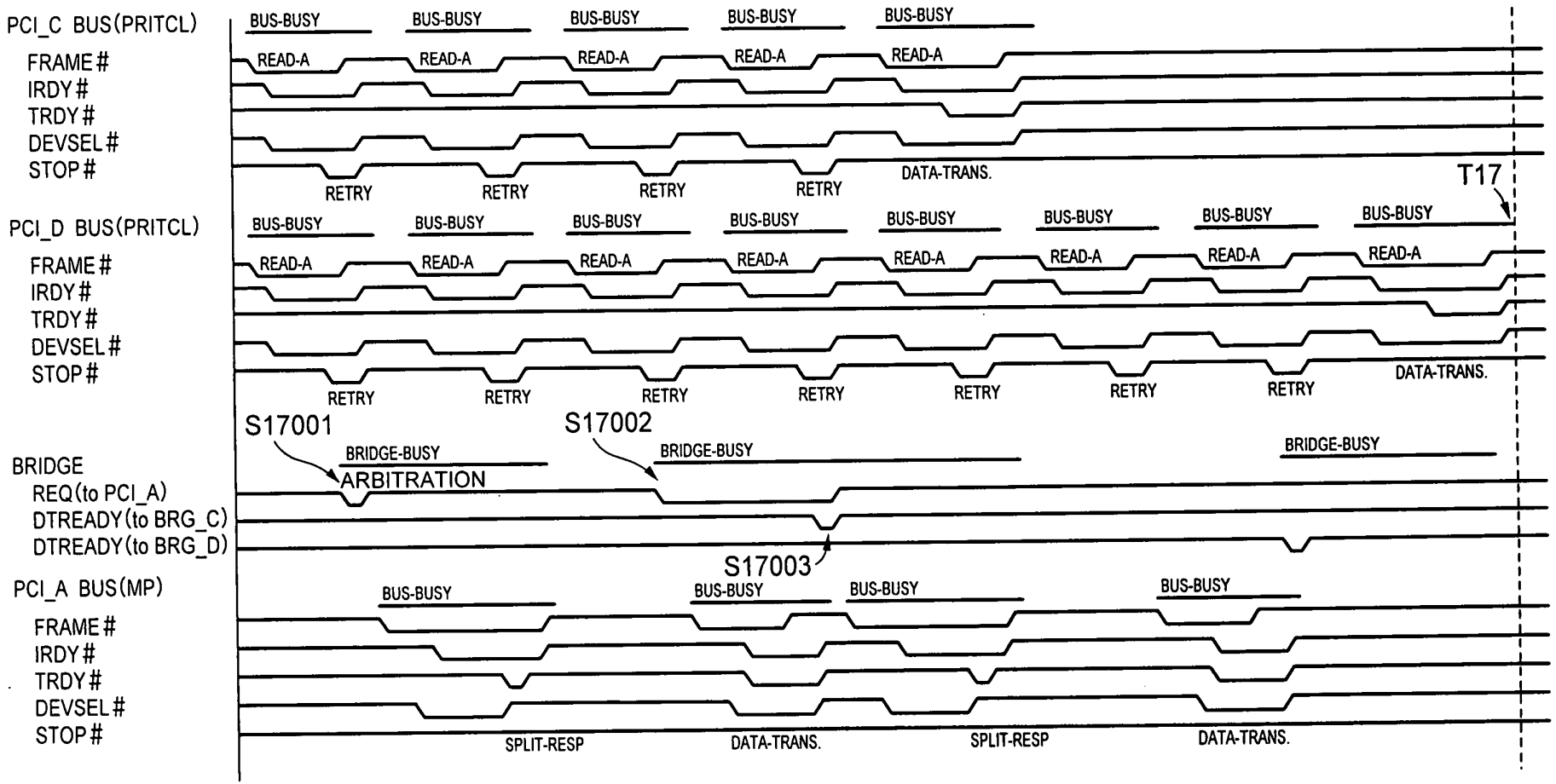

PCI_C BUS(PRITCL)
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
BUS-BUSY
READ-A
RETRY
DATA-TRANS.
T17
PCI_D BUS(PRITCL)
BRIDGE
REQ(to PCI_A)
DTREADY(to BRG_C)
DTREADY(to BRG_D)
S17001
S17002
S17003
BRIDGE-BUSY
ARBITRATION
PCI_A BUS(MP)
SPLIT-RESP

FIG. 18

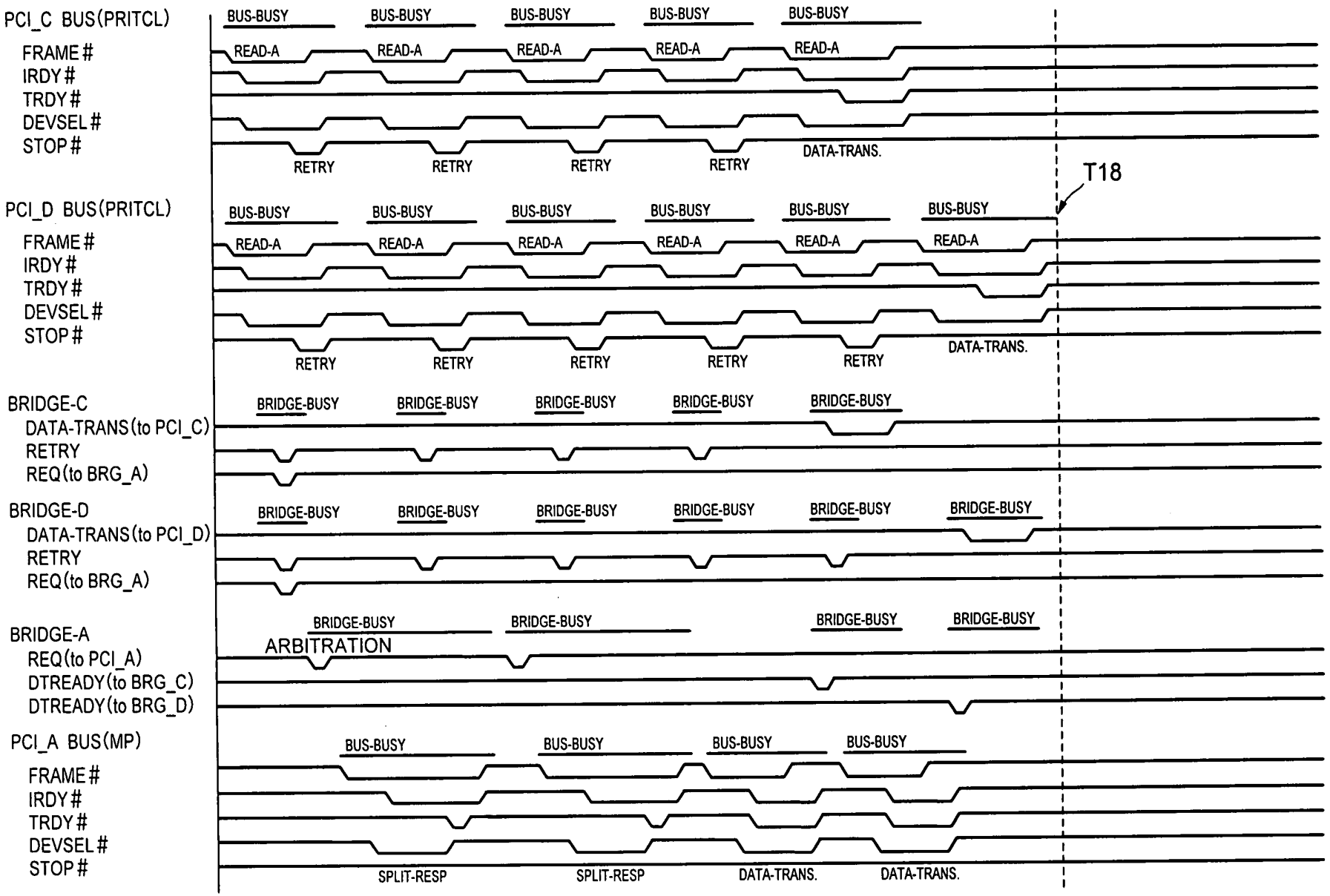

PCI_C BUS(PRITCL)
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
BUS-BUSY
READ-A
RETRY
DATA-TRANS.
T18
PCI_D BUS(PRITCL)
BRIDGE-C
DATA-TRANS(to PCI_C)
RETRY
REQ(to BRG_A)
BRIDGE-BUSY
BRIDGE-D
DATA-TRANS(to PCI_D)
BRIDGE-A
REQ(to PCI_A)
DTREADY(to BRG_C)
DTREADY(to BRG_D)
ARBITRATION
PCI_A BUS(MP)
SPLIT-RESP

FIG. 19

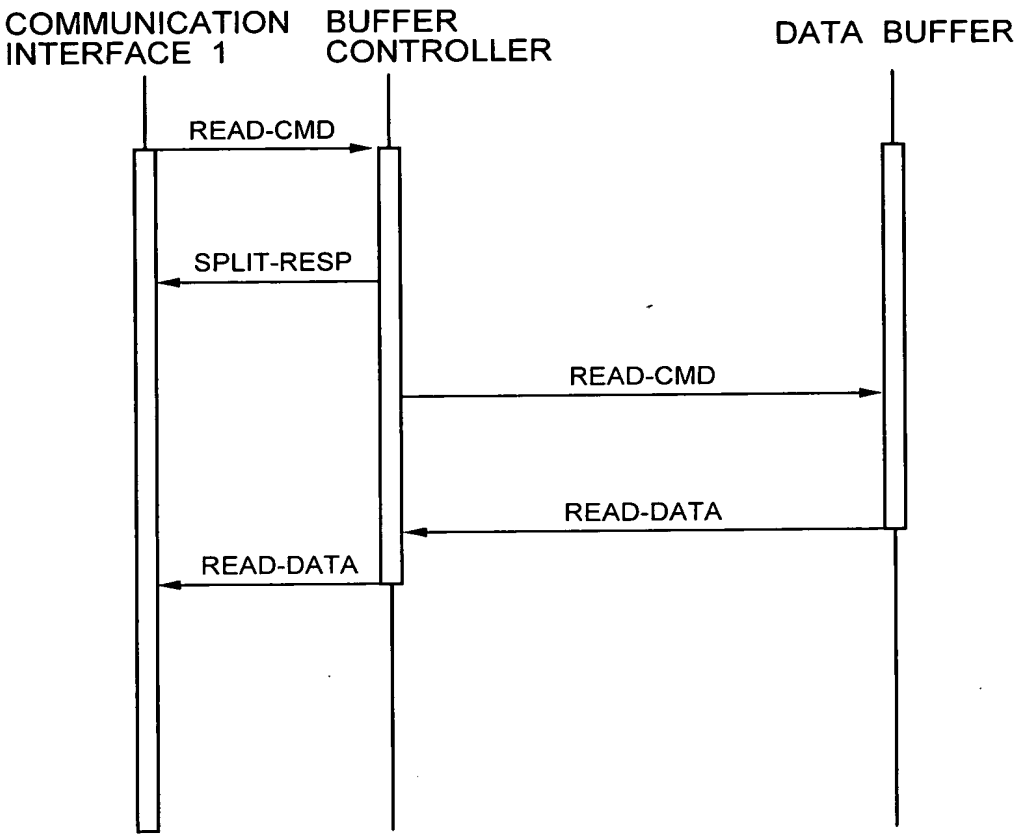
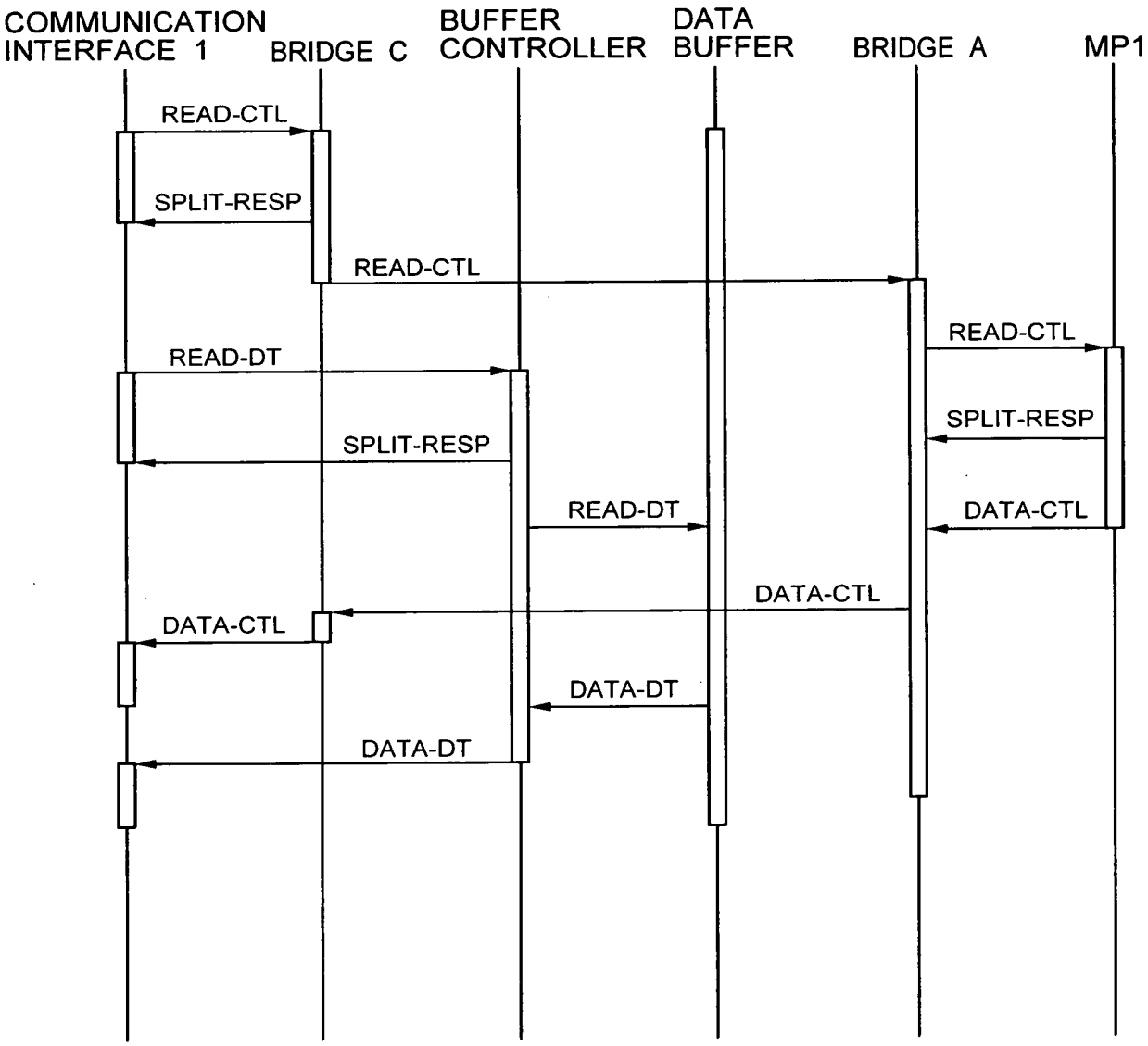

COMMUNICATION INTERFACE 1
BUFFER CONTROLLER
DATA BUFFER
READ-CMD
SPLIT-RESP
READ-CMD
READ-DATA
READ-DATA

FIG. 20


COMMUNICATION INTERFACE 1
BRIDGE C
BUFFER CONTROLLER
DATA BUFFER
BRIDGE A
MP1
READ-CTL
SPLIT-RESP
READ-CTL
READ-CTL
READ-DT
SPLIT-RESP
SPLIT-RESP
READ-DT
DATA-CTL
DATA-CTL
DATA-CTL
DATA-DT
DATA-DT